Hall Ticket Number:

Code No. : 15456 N

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) V-Semester Main Examinations, Jan./Feb.-2024

Microprocessors and Microcontrollers

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	Justify the significance of dividing the Physical memory of 8086μp into EVEN and ODD Address space and list the 8086 Pins involved in the operation?	2	3	1	1	1
2.	Draw the Write cycle timing diagram for 8086μp in minimum mode and explain the timing sequence.	2	2	1	1	1
3.	The size of a memory structure is 128MB and it is partitioned into equal size blocks of 64KB Determine the number of memory blocks and predict the starting and ending address of 4^{th} memory block-M4? (Assume starting block as M1)	2	3	2	2	1
4.	Configure the CWR of 8253 timer to generate a square wave on counter 2? (Assume default status for other bits suitably)	2	3	2	1	1
5.	Draw the RAM structure of 8051μc indicating the partitioning of 128byte space.	2	2	3	1	1
6.	Write a program for 8051μc to find the average of given 5 elements in an array loaded at the address starting from 50h?	2	2	3	2	1
7.	Draw the timing sequence of ADC 0808/0809 that determines the ADC conversion process.	2	3	4	1	1
8.	Write the configuration of IE register of 8051μc and explain the operation of each bit.	2	2	4	2	1
9.	Represent the interface diagram for DC motor with 8051μc.	2	1	5	1	1
10.	List any four industrial applications of 8051μc.	2	1	5	2	1
	Part-B (5 × 8 = 40 Marks)					
11. a)	Describe the process of latching of 20-bit address bus of 8086μp with a neat diagram.	3	2	1	1	1
b)	Explain the minimum mode configuration of 8086μp with a neat diagram.	5	2	1	1	1

Contd... 2

12. a)	Interface two ICs of SRAM of size 16K X 8 and two ICs of EPROM of size 8K X8 with 8086 µp? Select the address map suitably satisfying the 8086 µp architecture requirements?	5	4	2	3	1
b)	Describe the working of 8255 PPI with a neat architecture diagram.	3	2	2	1	1
13. a)	Define Addressing mode. Illustrate the addressing modes of 8051 µc with suitable example of each.	4	2	3	2	1
b)	Write a program to count the number of elements given in an array are divisible by 7? Assume the array has 5 elements and are loaded from an address 40h.	4	3	3	3	1
14. a)	Write a program to generate a square wave of 10KHz on pin P1.1 using Timer 0 in Mode-1. Assume Xtal freq= 11.0592MHz.	4	3	4	4	1
b)	Interface soil moisture sensor to 8051 µc with the help of ADC-0808 and send the received data from sensor to the serial monitor with 4800 baud rate.	4	3	4	4	1
15. a)	Write a program to interface 2*16 LCD with 8051 µc to display the message "MPMC EXTERNAL" in Line -1 starting from 3rd position.	4	2	5	4	1
b)	Write a program to interface stepper motor with 8051 µc to rotate in clockwise direction when the switch is ON and in Anticlockwise direction when the Switch is OFF. Assume the switch is connected at P2.1.	4	2	5	4	1
16. a)	Explain the process of Interrupt response sequence in 8086µp with a suitable diagram.	4	1	1	2	1
b)	Explain the operation of 8257 DMA controller with a suitable interface diagram around 8086µp.	4	1	2	1	1
17.	Answer any ***two*** of the following:					
a)	Explain the architecture of 8051 µc with a neat diagram.	4	1	3	1	1
b)	Write a program to transmit the string "VASAVI "over the serial port of 8051 µc at a baud rate of 9600? (Assume Xtal freq= 11.0592Mhz)	4	3	4	2	1
c)	Interface a 4X3 Matrix Hexadecimal Keypad with 8051 µc and write a program to display the key pressed on 7-segment display.	4	3	5	3	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	38.75%
iii)	Blooms Taxonomy Level – 3 & 4	41.25%

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